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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): Fischer 46-3

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Application Number	Filed
10/719,645	11/21/03

First Named Inventor: Fischer et al.

Art Unit	Examiner
2627	Glenda P. Rodriguez

Applicant requests review of the final rejection in the above-identified application No amendments are being filed with this request

This request is being filed with a notice of appeal

The review is requested for the reason(s) stated on the attached sheet(s)
Note: No more than five (5) pages may be provided

I am the

- [ ] applicant/inventor
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3 73(b) is enclosed (Form PTO/SB/96)
- [X] attorney or agent of record Registration number 36,597
- [ ] attorney or agent acting under 37 CFR 1 34 Registration number if acting under 37 CFR 1 34 _____

Kevin M. Mason
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Telephone number

February 26, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1 14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS **SEND TO: Mail Stop AF, Commissioner for Patents, P O Box 1450, Alexandria, VA 22313-1450**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Fischer et al.
Case:	46-3
Serial No.:	10/719,645
Filing Date:	November 21, 2003
Group:	2627
Examiner:	Glenda P. Rodriguez
Title:	Long Hold Time Sample and Hold Circuits

MEMORANDUM IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The present invention and prior art have been summarized in Applicants' prior responses.

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 through 20 are presently pending in the above-identified patent application. Claims 1, 7, 8, and 13 are rejected under 35 U.S.C. §102(e) as being anticipated by Luo (United States Patent Number 6,111,467), claims 3, 4, 10 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Luo in view of Beauducel et al. (United States Patent Number 4,352,070), claims 6 and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Luo in view of Mills et al. (United States Patent Number 5,172,117), and claims 2, 5, and 9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Luo in view of Sandusky et al. (United States Patent Number 5,825,571). The Examiner indicated that claims 14-20 are

allowed.

ARGUMENTS

Independent Claims 1 and 8

Independent claims 1 and 8 are rejected under 35 U.S.C. §102(e) as being anticipated by Luo. In particular, the Examiner asserts that Luo discloses a sample and hold circuit. Among other features, the Examiner asserts that Luo also discloses (i) at least one capacitive element for retaining a charge, said at least one capacitive element connected to a node between said input and said output (citing element C1 in FIG. 1); (ii) at least one output switch for selectively connecting said at least one capacitive element to said output (citing element S3 of FIG. 1); and (iii) an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage (FIG. 1: element 11; col. 3, lines 50-64).

Applicants note that, regarding element C1, Luo teaches that,

> continuing to refer to FIG. 1 and FIG. 2, **during quarter period 2** switch S1 connecting the first transconductor 10 to the operational amplifier 11 is open, and switch S2 connecting the sample and hold capacitor C2 to the output of the operational amplifier 11 is closed allowing capacitor C2 to be charged up to a voltage equal to that on capacitor C1. **Switches S4a and S4b remain closed.** Switch S6 is closed to discharge the voltage on the parasitic capacitance at the output of the transconductor 10. **All other switches are open during quarter period 2.**
>
> Continuing to refer to FIG. 1 and FIG. 2, **during quarter period 3** switch S0 is closed to discharge the voltage on the feed back capacitor C1. Switch S5a is closed to connect input voltage k_2 V_R to the input of the transconductor 10 and **switch S5b is closed to connect a voltage reference $-V_R$ to the (+) input terminal of the current summing operational amplifier 11**. Switch S6 remains closed to discharge the voltage on the parasitic capacitance at the output of the transconductor 10. **All other switches are open during quarter period 3.**
>
> Continuing to refer to FIG. 1 and FIG. 2, during quarter periods 4 and 5 switches S1, S5a and S5b are closed, and all other switches are open. The feedback capacitor C1 is charged for one half clock period by the output of the transconductor 10 from the reference voltage $-V_R$ to a voltage $-V_y$. During quarter period 6 switches S5a and S5b remain closed and S3 is closed allowing a voltage equal to that on capacitor C1 to be put onto capacitor C3. Switch S6 is closed to discharge the capacitance on the parasitic capacitance at the output of the transconductor 10, and all other switches are open.
> (Col. 4, lines 23-53; emphasis added.)

Luo teaches that *switch S4b is closed and switch S5b is open during quarter 2*, and that *switch S4b is open and switch S5b is closed during quarter 3*. Thus, Luo actually *teaches away* from the present invention by teaching to ***not*** *limit* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*. Independent claim 1 requires an amplifier connected to said node, *wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage*. Independent claim 8 requires *limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element*.

Thus, Luo does not disclose or suggest an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, as required by independent claim 1, and does not disclose or suggest limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element, as required by independent claim 8.

Additional Cited References

Beauducel was also cited by the Examiner for its disclosure of a resistor placed in parallel as disclosed in the sample and hold circuit of FIG 4 (R_1). Although Beauducel is directed to a sample and hold circuit, Beauducel does *not* disclose or suggest the feature of *limiting* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*.

Thus, Beauducel et al. do not disclose or suggest an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, as required by independent claim 1, and does not disclose or suggest limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element, as required by independent claim 8.

Mills was also cited by the Examiner for its disclosure of a sample and hold circuit in which its hold time is 200 microseconds. Applicants note that Mills is directed to an analog to digital signal converter that includes an integrator and a sample and hold circuit. Mills does *not*, however, disclose or suggest the feature of *limiting* a voltage drop across at least one of

the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*.

Thus, Mills et al. do not disclose or suggest an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, as required by independent claim 1, and does not disclose or suggest limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element, as required by independent claim 8.

Sandusky was also cited by the Examiner for its disclosure of a sample and hold circuit for a preamplifier in a disk drive. Applicants note that Sandusky is directed to a circuit for input switching for a read channel. Sandusky does *not*, however, disclose or suggest the feature of *limiting* a voltage drop across at least one of the input and output switches *to an offset voltage of an amplifier connected to the capacitive element*.

Thus, Sandusky et al. do not disclose or suggest an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, as required by independent claim 1, and does not disclose or suggest limiting a voltage drop across at least one of said input and output switches to an offset voltage of an amplifier connected to said at least one capacitive element, as required by independent claim 8.

Dependent Claims 2-7, 9-13 and 15-20

Dependent claims 7 and 13 were rejected under 35 U.S.C. §102(e) as being anticipated by Luo, claims 3, 4, 10 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Luo in view of Beauducel et al., claims 6 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Luo in view of Mills et al., and claims 2, 5, and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Luo in view of Sandusky et al.

Claims 2-7, 9-13, and 15-20 are dependent on claims 1, 8, and 14, respectively, and are therefore patentably distinguished over Luo, Beauducel et al., Mills et al. and Sandusky et al., alone or in combination, because of their dependency from independent claims 1, 8, and 14 for the reasons set forth above, as well as other elements these claims add in combination to their base claim. The Examiner has already indicated that claims 15-20 are allowed.

For example, claims 3, 10 and 16 require that at least one of the input and output switches has a leakage effect represented by a resistor in *parallel* with the input or output switch and a voltage drop across the resistor is limited to the offset voltage. The Examiner asserts that FIG. 4 of Beauducel et al. teaches a resistor, R_1, placed in parallel. Applicants note, however, that resistor, R_1, is in *series* with the current through switch I_1. If the switch I_1 is in an open position, there is no current from the amplifier A_1 through the resistor R_1.

All of the pending claims, i.e., claims 1-20, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully,

Date: February 26, 2007

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